Optimizing of Metal-Insulator-Metal Capacitors Performances by Atomic Layer Deposition: Advancing Production Efficiency and Throughput

Doctorant·e
IHARA Kou

Direction de thèse
LABBE Christophe (Directeur·trice de thèse)
CARDIN Julien (Co-directeur·trice de thèse)

Date de la soutenance
11/07/2024 à 09:00

Lieu de la soutenance
Salle de Thèse

Rapporteurs de la thèse
MARCO DE LUCAS MARIA DEL CARMEN Professeur des universités UNIVERSITE BESANCON FRANCHE COMTE
MUNOZ-ROJAS DAVID Directeur de recherche Universite Grenoble Alpes

Membres du jurys
BLANQUET ELISABETH, Directeur de recherche, Universite Grenoble Alpes
CARDIN Julien, Ingénieur de recherche, Université de Caen Normandie
LABBE Christophe, Maître de conférences, Université de Caen Normandie
MARCO DE LUCAS MARIA DEL CARMEN, Professeur des universités, UNIVERSITE BESANCON FRANCHE COMTE
MECHIN Laurence, Directeur de recherche au CNRS, ENSICAEN
MUNOZ-ROJAS DAVID, Directeur de recherche, Universite Grenoble Alpes

Abstract
As semiconductor technology progresses, the need to overcome the limitations of shrinking device sizes is considered paramount. While Moore’s law has guided this evolution over the past five decades, the constraints of the active components are now obvious as manufacturing processes approach the atomic scale. More Than Moore's approach has emerged to address this, emphasizing the integration and miniaturization of heterogeneous chips to enable the stacking of diverse system functionalities. However, integrating passive components poses significant challenges due to their production via disparate processes. Addressing this challenge, Murata Integrated Passive Solutions invented the Passive Integrated Connecting Substrate (PICS) technology, facilitating the integration of silicon-based passive components into 3D structures. The latest iteration, PICS5, leverages an anodic aluminum oxide template and Metal-Insulator-Metal stack deposition via atomic layer deposition. This thesis contributed to the ongoing refinement of PICS5 technology by enhancing the properties of 3D capacitors and exploring the potential of high-k dielectric materials (Nb_2O_5). This research aimed to optimize component performance and anticipate future challenges in semiconductor innovation by clarifying the nuances of thin film deposition processes and ALD equipment conditions.